Claims

[c1] What is claimed is:

1.A pulse width control system comprising:

a serial transmission line for receiving serial data signals;

a differential pair having a first transistor and a second transistor, the first and second transistors being connected to the transmission line for respectively producing a positive data signal and a negative data signal, the first transistor being controlled by a first control signal and the second transistor being controlled by a second control signal, a differential data signal being produced by subtracting the negative data signal from the positive data signal;

a first delay control cell connected to the first transistor for delaying the first control signal;

a second delay control cell connected to the second transistor for delaying the second control signal;

wherein delay times caused by the first and second delay control cells to delay the first and second control signals are adjusted to ensure that all data pulses of the differential data signal have uniform width.

[c2] 2.The system of claim 1 wherein when a status of the serial transmission line remains in transmit mode, the first and second delay control cells generate a first delay time.

[c3] 3.The system of claim 2 wherein when a status of the serial transmission line switches from idle mode to transmit mode, the first and second delay control cells generate a second delay time.

[c4] 4.The system of claim 3 wherein the second delay time is larger than the first delay time.

[c5] 5.The system of claim 3 wherein the second delay time is generated to delay exactly one data pulse after the switch from idle mode to transmit mode.

[c6] 6.The system of claim 1 wherein the first and second delay control cells comprise controllable resistor strings for providing delay times.

[c7] 7.The system of claim 1 wherein the first and second delay control cells

comprise controllable capacitor arrays for providing delay times.

[c8] 8.The system of claim 1 wherein the first and second delay control cells comprise logic circuitry, and delay times are produced by propagation delays of the logic circuitry.

[c9] 9.The system of claim 1 wherein the first and second delay control cells each comprise a control transistor, and delay times are produced by varying voltage levels of signals that control the control transistors in order to change channel widths of the control transistors.